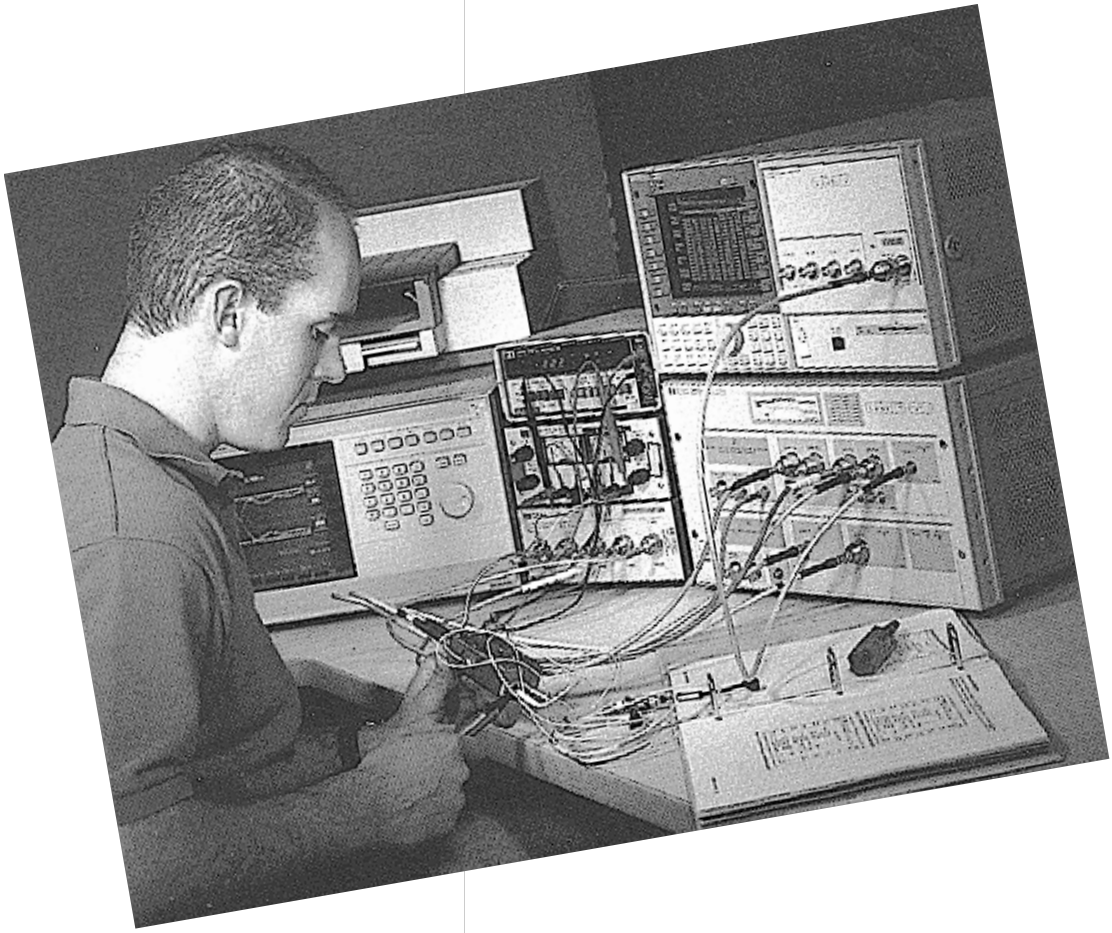
Technique

HEWLETT PACKARD
Expanding Possibilities

HP **71612A/B** 12 Gb/s error performance analyzer



Locating errors in Gigabit transmission systems and components

Conventional error performance analysis

To test a digital system, the input is stimulated by a test pattern. Usually this is a Pseudo Random Binary Sequence (PRBS), though other specific stress patterns (referred to as user-defined word patterns) may be used to explore limits of performance. Typical stress patterns might include long runs of '0s' to test clock recovery, or patterns with alternate periods of high and low mark ('1') density to check storage effects in optical transmitters and receivers which may respond to the average mean level in a data signal.

For telecommunications and datacommunications transmission systems, the object is to simulate the random traffic experienced under normal operating conditions. The problem with a truly random signal is that an error detector will have no means of knowing the actual bit values that were transmitted and therefore no way of detecting errors. Instead, a pseudo random signal is used, which means that it has almost all the statistical characteristics of a true random signal, and appears as such to the item under test, while in fact being completely deterministic and therefore predictable by the error detector. A range of maximal length PRBS patterns are normally used for testing in this way. At the error detector, the output of the system under test is compared bit by bit with a locally generated, error-free reference pattern as shown in Figure 1.

Bit error ratio (BER)

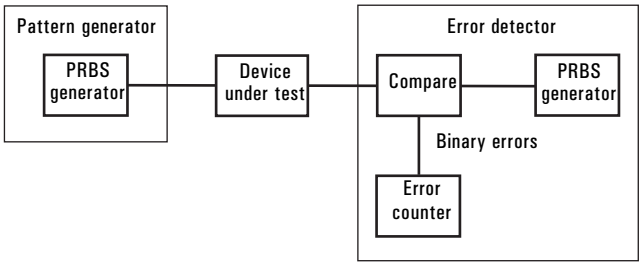


Figure 1. Conventional out-of-service BER measurement

The probability of an error in any transmitted bit can be expressed in various ways, the most common of which is Bit Error Ratio (BER):

$$\text{BER} = \frac{\text{Number of errors (in the measurement interval)}}{\text{Number of bits transmitted (in the same interval)}}$$

Clearly the result will have a random statistical variance from the long-term mean error ratio dependent on the size of the sample taken – in this case the number of errors counted. This means that for a low error rate the measurement must take place over a relatively long period. In the past, BER was the standard measure of digital performance but as it gives no indication of when or how, errors occur, it is of limited value.

Errored seconds (ES)

Measurements such as error seconds (ie, a one second interval in which one or more errors occur) are often used in addition to the BER measurement in establishing system performance and for analyzing faults.

Error-free seconds (EFS)

Error performance analyzers show the distribution of errors with time by simultaneously counting the number of errored and error-free seconds. This gives limited indication of errors associated with pattern characteristics, as the pattern's sequence is not synchronized to the measurement interval. Depending on the pattern length and bit rate, the number of pattern repetitions can vary widely in any time interval.

Bit errors,
Logic errors

To obtain an absolute measure of performance, every single bit of the transmitted signal must be measured. This is normally done as shown in Figure 1. The receiver generates an identical pattern and, once synchronized with the transmitted pattern, the two patterns are compared. Any difference constitutes a binary (bit or logic) error. Various length and types of pattern can be used to fully explore the networks susceptibility to pattern dependent errors. PRBS patterns are often used since they closely approximate the characteristics of live traffic. Shorter patterns with varying densities of 1s and 0s are used to test for pattern sensitivity. These measurements are normally performed by an error performance analyzer.

When evaluating system performance the nature of received errors are analyzed in an attempt to diagnose which part of the system is causing these errors. However the failure mechanism may not be obvious due to the way that errors may be received. The effects of the error distribution can also be very important. For example, in the scenarios below, the error count and BER are the same.

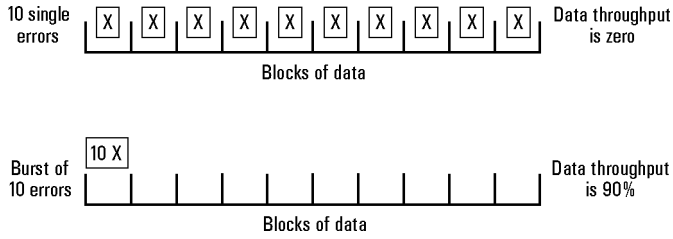


Figure 2. Alternative distributions of error

Severely errored seconds (SECs)

The error distribution can be investigated in the time domain, but independent of pattern, by counting severely errored seconds (ie, a one second interval when BER $\geq 1 \times 10^{-3}$). Counting severely errored seconds allows the operator to identify bursts of errors. This task is made easier as modern error performance analyzers can often display different interval measures, for example errored milliseconds. If the occurrence of these bursts are time-stamped on a printout of measurement results this can help the operator establish if the error cause is correlated with a real-time event. This measurement technique is mainly used on out-of-service links.

This analysis technique may be improved if the error performance analyzer is able to measure and display the number of 1s that have erroneously become 0s, and 0s that have erroneously become 1s. This additional information may point to the underlying impairment mechanism, giving the user some indication of the error source.

Error location analysis

Systematic errors
Pattern-dependent errors

The HP 71612A/B 12 Gb/s error performance analyzer offers an important innovation in error diagnostics: error location analysis. This feature is useful when analyzing systematic or pattern-dependent errors (for example, errors caused by incorrect bias of a laser on an optical transmission system). Error location analysis allows the location of errors in the received signal to be analyzed in terms of their position in the pattern. Error location analysis can be used on any pattern stored in the HP 71612A/B analyzer's pattern memory (PRBS pattern up to $2^{15} - 1$ loaded into RAM, mark density, zero substitution patterns or any user pattern selected from the instrument or from a storage disk).

The HP 71612A/B analyzer has a pattern editor which can be used to copy, "cut and paste", then save patterns to RAM. Patterns are either created from scratch or copied into RAM from one of the standard patterns supported (for example, PRBS 2^{13}). Patterns may also be created on your PC using either HP's pattern constuction program or one written yourself.

Error location analysis consists of a set of three measurements.

Bit BER

1. Bit BER: A user may specify any bit in a pattern (the bit error address) and perform BER measurements upon only that bit. This aids in identifying systematic errors causing a specific bit to change value. If the error distribution is constant over time, this feature allows the operator to 'step through' each bit in the pattern and construct a picture of the error distribution. This task can be automated by controlling the HP 71612B analyzer over the HP-IB (IEEE-488).

Block BER

2. Block BER: BER measurements are performed on a block (range of bits) within a user defined pattern. The block length must be a multiple of 32 and is specified by a start location and a block length. This feature is useful when locating the cause of errors which affect a block, or for performing measurements on only part of a pattern. For example, the payload or overhead elements of an SDH or SONET frame could be measured as required.

Error location capture

3. Error location capture: To detect systematic errors, error location capture searches for errored bits in a defined, continually-repeated pattern. On starting the error location capture measurement, the error detector finds the position of the first errored bit in the pattern (ie, first errored bit after the current Bit BER setting). The address of this bit becomes the bit error address. This address is now displayed along with the surrounding bit pattern and is highlighted. The error detector then automatically measures the Bit BER for this bit error address in the repeats of the pattern.

To find the next bit error address in the pattern, the user resumes the error location capture process. This time, the error detector finds the next errored bit in the pattern after the initial bit error address and a new Bit BER measurement is initiated. The analyzer steps to the next bit error address each time that error location capture is started.

In figure 3, errors present in the pattern are shown in positions marked (1), (2) and (3). When error location capture is initiated, a Bit BER measurement is made at bit error address (1) once the error is located. Initiating error location capture a second time allows the second error to be detected and the analyzer moves the bit error address to the bit at position (2). If error location capture is initiated again, the bit error address moves to position (3), and so on.

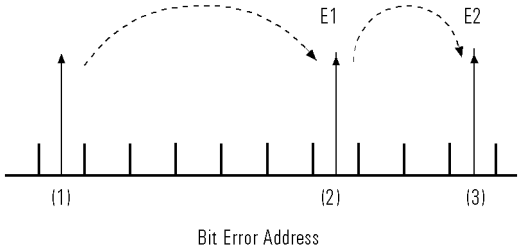


Figure 3. Error location capture in action

If the error rate of the captured bit remains above the overall average over a period of time it is a systematic error. This helps to discriminate between random and systematic errors, helping to identify the error source.

Note: Error location capture may also be used in conjunction with an oscilloscope.

Error location analysis is a very powerful tool when diagnosing systematic errors. The following three examples help to explain how the measurement works.

Example 1
A one million bit sequence is transmitted repetitively. If the same bit is errored every time (ie, error rate of that bit is one) then error location will find the errored bit every time assuming that the residual error rate is zero.

Example 2
If the systematic errors present in each bit location are as shown in Figure 4, with a zero residual error rate, what will error location capture? The bit locations which have a BER of 1×10^{-3} are most likely to be found but the other errored bit locations will statistically have less chance of being found. In this instance only bits with a 1×10^{-3} error rate can be investigated. Once these errors have been eliminated, the bits with lower error rates can be found.

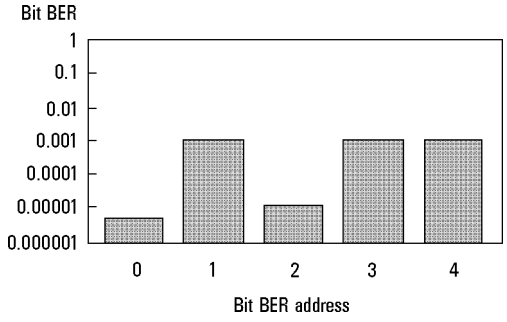


Figure 4: Errors present in each bit location

Notes:
1. Errors at bits 0 or 2 may be found, but are proportionately less likely to be captured.
2. Single-shot bit errors can be captured provided that a single-shot errored bit is first to occur following capture indication.

Example 3
Identifying systematic errors is more complicated in the presence of random errors. For example, if the random error rate is 1×10^{-6} and the bit sequence is one million bits long then there will be one error every pattern repetition. If the signal is transmitted at 10 Gb/s there will be 10,000 random errors every second. If the largest systematic error rate in any bit is 1×10^{-3} then there will be one error every 1,000 pattern repetitions. If transmitted at 10 Gb/s there will be 10 systematic errors every second. In this case, it would be difficult to analyze the systematic errors since the random error rate is higher than the systematic error rate. To analyze systematic errors effectively, the residual random error rate should be significantly lower than the systematic bit error rate.

Bit and Block BER can be analyzed using a successive approximation technique in order to "home-in" on problem bit sequences within a pattern. The pattern may be scanned initially using a block length equal to half the pattern length, BER being measured over each half in turn. Any errored half pattern found may be scanned again with the block length halved and so on. In this way a profile of the BER with respect to pattern can be built up with a resolution down to the minimum block size of 32 bits. This feature could be used to analyze a block of data which is used to simulate a SONET or SDH frame or when errors in only part of the pattern are of interest. Where the pattern is simulating a frame structure normally used by the system under test, the block start and length can be used to see only the portions of the frame which are of interest.

Using an oscilloscope to display errored bits

The pattern generator's trigger output on the HP 71612A/B analyzer may be used to trigger an oscilloscope to display errored bits and adjacent parts of the pattern. As the entire user pattern is stored in RAM, the errored address can be cross referenced to any bit in the pattern and the user pattern displayed on the analyzer's display. In this manner, the operator may examine the pattern around the errored bit(s) and acquire information concerning the pattern dependencies which can cause systematic errors. Alternatively the operator can choose to examine an errored bit on the oscilloscope. This may help to identify waveform/pulse distortion or intersymbol interference.

To display errored bits on an oscilloscope, the power of error location capture is combined with the power of the pattern trigger. For best results compensate for cable delays prior to any measurement.

One method of compensating for cable delays is to produce a RAM pattern which has a zero-to-one transition in the pattern at bit 0 assuming that the pattern trigger bit is set to bit zero. This pattern should be the same length as the pattern used for testing. The pattern should be structured to permit the zero-to-one transition to be easily identified. For example, the following pattern could be used as the zero-to-one transition can be easily identified.

. . . .00000001111111 . . . .
↑
bit 0

If the device under test will not tolerate long runs of ones and zeros then use another distinguishable pattern, such as a run of 010101 and a run of 001100110011. To find the errored transition on the oscilloscope screen, implement a binary search technique, using the trigger position. Confirm the correct transiton by toggling the bit in question. If the correct bit is being displayed on the oscilloscope it should also toggle. Increase the timebase resolution until the zero-to-one transition becomes visible.

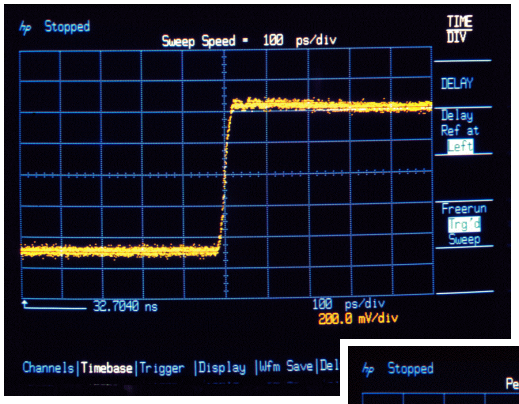


Figure 5. Oscilloscope showing zero-to-one transition

Increase the delay to move the pulse to the left-hand side of the oscilloscope display and reduce the timebase resolution down to achieve the desired resolution. The zero-to-one transition should now be displayed in the center of the oscilloscope display (Figure 5). The cable delays are now compensated for and the bit number selected by the trigger will now be displayed in the center of the oscilloscope display.

Note: If you encounter a timebase/delay range conflict in the oscilloscope which makes it difficult to display the errored bit with sufficient resolution, move the pattern trigger bit until the errored bit can be displayed on the oscilloscope.

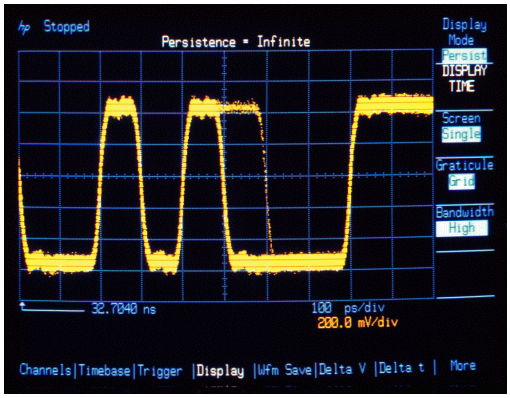


Figure 6. Observed systematic error

Using error location analysis, the bit error address is found. The trigger mode should be set to pattern and the captured bit error address entered as the "PG TRIG BIT" value. The bit number selected by the trigger will be shown in the center of the oscilloscope display (Figure 6). Note that it may be necessary to increase the oscilloscope display persistence to observe the errors occurring at that bit. Alter a bit in the pattern to verify the correct part of the pattern is being displayed.

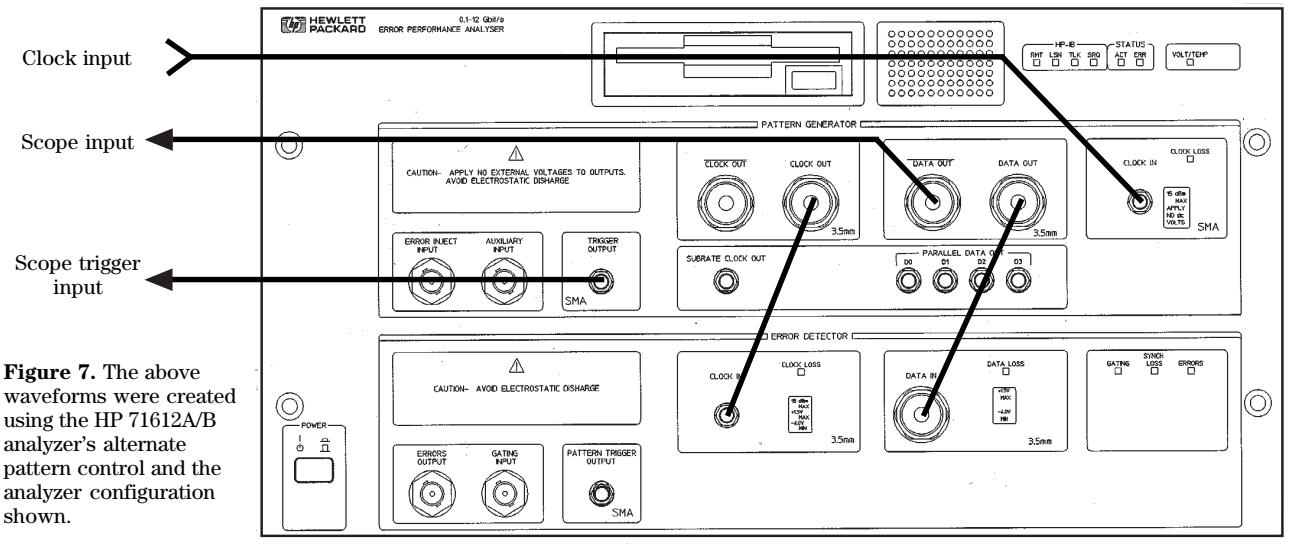


Figure 7. The above waveforms were created using the HP 71612A/B analyzer's alternate pattern control and the analyzer configuration shown.

HEWLETT PACKARD
Expanding Possibilities

Pattern sampling

The RAM in the error performance analyzer is organized 256 bits wide. This determines how patterns are stored and how some features, such as triggering, work.

Within the error performance analyzer, patterns are replicated in RAM until they are a multiple of 256 bits. Patterns which are already a multiple of 256 bits need no replication, other patterns are replicated as many as 256 times. For example all odd length patterns are replicated 256 times.

When using error location analysis features, the analyzer will only perform measurements on the customer defined pattern. Although the instrument repeats the pattern in RAM until it is a multiple of 256 bits, any additional bits added by repeating the pattern are not displayed as part of the measurement. This replication process is transparent to the user. It does affect the sampling rate in bit and block BER. Error location analysis is only performed on the first instance of the repeated pattern. Where single-shot bit errors are to be located, the pattern length should be a multiple of 256 to give continuous measurements. Creating patterns that are multiple of 256 bits is easily accomplished using the block copy feature found in the user pattern editor.

Hewlett-Packard manufactures the HP 71612A/B analyzer under a quality system approved to the international standard ISO 9002 plus TickIT (BSI Registration Certificate No FM 10987).

For more information about Hewlett-Packard test & measurement products, applications, services, and for a current sales office listing, visit our web site, http://www.hp.com/go/tmdir. You can also contact one of the following centers and ask for a test and measurement sales representative.

United States:
Hewlett-Packard Company
Test and Measurement Call Center
P.O. Box 4026
Englewood, CO 80155-4026
1 800 452 4844

Canada:
Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
1 877 894 4414

Europe:
Hewlett-Packard
European Marketing Centre
P. O. Box 999
1180 AZ Amstelveen
The Netherlands
(31 20) 547 9999

Japan:
Hewlett-Packard Japan Ltd.
Measurement Assistance Center
9-1, Takakura-Cho, Hachioji-Shi
Tokyo 192-8510, Japan
Tel: (81) 426 56-7832
Fax: (81) 426 56-7840

Latin America:
Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive, 9th Floor
Miami, Florida 33126
USA
(305) 267 4245/4220
Fax: (305) 267-4288

Australia/New Zealand:
Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
Tel: 1 800 629 485 (Australia)
Tel: 0800 738 378 (New Zealand)
Fax: (61 3) 9210 5489

Asia Pacific:
Hewlett-Packard Asia Pacific Ltd.
17-21/F Shell Tower, Times Square
1 Matheson Street, Causeway Bay
Hong Kong
Tel: (852) 2599 7777
Fax: (852) 2506 9285

Printed in USA
Data subject to change
5968-2811E (02/99)

CE